oxygen gas;

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

REMARKS

The Office Action of **August 14, 2002** has been received and its contents carefully noted. Applicants respectfully submit that this response is timely filed and fully responsive to the Office Action. Claims 1-14 and 29-37 were pending in the present application prior to the aforementioned amendment. By the above amendment, claims 1, 6, 11, 30, and 34 are amended to more clearly define the subject matter which the Applicants regard as the invention. Because the amended claim language is supported at least on page 25, line 3, the Applicant submit that no issue of new matter is raised by this amendment. Accordingly, claims 1-14 and 29-37 are still pending in the present application and, at least for the reasons set forth below, are believed to be in condition for allowance.

With regard to the Examiner's rejections of:

Claims 1-4, 6-9, 30-33, under 35 U.S.C. 103(a), as being obvious in view of the teachings of Misawa et al ('279) in view of applicant's Admitted prior art (APA) and the Ang et al (1993) article,

Claims 11-13, 29 and 34-37, under 35 U.S.C. 103(a), as being obvious in view of the teachings of Misawa et al ('279) in view of applicant's Admitted prior art (APA), the Ang et al article and Wolf et al, "Silicon Processing…" pages 183-184 (1986),

Claims 1-4, 6-9, 11-13, 29, 30-37, under 35 U.S.C. 103(a), as being obvious in view of the teachings of Misawa et al ('279) in view of applicant's Admitted prior art (APA), Roy ('701) and Wolf et al, "Silicon Processing…" pages 57-58 (1986),

Claims 5 and 10, under 35 U.S.C. 103(a), as being obvious in view of the teachings of Misawa et al ('279) in view of applicant's Admitted prior art (APA), the Ang et al article and JP ('030), and

Claim 14, as being obvious in view of the teachings of Misawa et al ('279) in view of applicant's Admitted prior art (APA), the Ang et al article, Wolf et al, "Silicon Processing..." pages 183-184 (1986) and JP ('030)

each of these rejections is respectfully traversed.

Specifically, in response to these rejections, the Applicants have amended claims 1, 6, 11, 30, and 34 to recite that a gate insulating film of a TFT is formed by using TEOS at a temperature of 200 to 400° C. (See the specification, page 25, line 3). In the embodiment where a gate insulating film of a TFT is formed by using TEOS, the formation should be performed at a lower temperature because a TFT is generally formed over a glass substrate. However, an insulating film formed by using TEOS at a lower temperature is **not** suitable for a gate insulating film because the film contains a significant number of carbon atoms and hydrocarbon groups which form clusters and trap centers and provides too high an interfacial density (See the specification, page 4, lines 1-13). In the light of the above, the present invention suggests irradiating an intense light on a gate insulating film which is formed by TEOS at a lower temperature in order that the interfacial density is sufficiently reduced.

Referring to Roy, an insulating film formation process by using TEOS is performed at a higher temperature in the range of 625-750° C. (column 4, lines 2-11). Also, Wolf et al. teaches that a gate insulating film formation process by using TEOS is performed at a higher temperature in the range of 650-800° C. (page 184). These cited references do not teach or disclose forming an insulating film by using TEOS at a lower temperature as mentioned in the present invention, and further do not suggest or teach applying such a gate insulating film of a TFT by a process including irradiating an intense light to reduce the interfacial density.

In point of fact, each of Roy (column 2, lines 9-25; column 3, lines 9-43) and Wolf et al (page 184) teach just the opposite of the claimed low temperature TEOS deposition of the gate insulating film with intense radiation by noting that <u>high</u> temperature TEOS deposition overcomes the interfacial density problem (Roy) and provides excellent conformability (Wolf et al). One of ordinary skill in the prior would not have been taught to perform the claimed steps of forming the gate insulating film, under low temperature TEOS deposition with intense radiation, since Roy teaches that the problem of interfacial density is improved by <u>high</u> temperature TEOS deposition and since Wolf et al teach that high temperature deposition provides benefits in conformation of the insulating film on the substrate. To combine the teachings of Roy and Wolf et al with those of Misawa et al as asserted by the Examiner would not yield the claimed invention since such a combination would teach to provide a <u>high</u> temperature TEOS deposition to eliminate the interfacial density problem which would then <u>not</u> require the use of intense radiation, allegedly taught by the Ang et al article, to reduce the interfacial density, i.e., <u>the intense radiation step would be eliminated by the Examiner's proposed combination</u>. Therefore, one of ordinary skill in the prior art is not provided with any motivation by the cited references or the Examiner to combine **both** <u>low temperature TEOS deposition</u> and <u>the intense radiation step</u> presently claimed, and even if combined as the Examiner alleges the proposed combination would not yield the process as claimed since the intense radiation step would no longer be needed. Consequently, a *prima facie* case of obviousness has not been established, and the Applicants urge that the rejections, under § 103, of claims 1-14 and 29-37 have been set forth in error and, further, respectfully request that the rejections be withdrawn.

CONCLUSION

Having responded to all rejections set forth in the outstanding Office Action, it is submitted that claims 1-14 and 29-37 are in condition for allowance. An early and

favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicant's undersigned representative.

Lastly, it is noted that a separate Extension of Time Petition (two months) accompanies this response along with a check in payment of the requisite extension of time fee. However, should that petition become separated from this Amendment, then this Amendment should be construed as containing such a petition. Likewise, any overage or shortage in the required payment should be applied to Deposit Account No. 19-2380 (740756-2064).

Respectfully submitted,

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Marked-up copy of Amended Claims

Please amended claims 1, 6, 11, 30 and 34 as follows.

1. (Four Times Amended) A method for manufacturing a [semiconductor device] <u>thin film transistor</u> comprising the steps of:

forming a semiconductor film comprising amorphous silicon over a substrate;

crystallizing said semiconductor film by irradiating a laser light;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film <u>comprising silicon oxide</u> on each of said first and second semiconductor islands by a vapor phase deposition <u>using TEOS at a temperature of 200 to 400° C.</u>;

irradiating an intense light to said insulating film [in an atmosphere comprising an oxygen gas]; <u>and</u>

forming a gate electrode on said insulating film[;]<u>.</u>

[introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.]

6. (Four Times Amended) A method for manufacturing a [semiconductor device] <u>thin film transistor</u> comprising the steps of:

forming a semiconductor film comprising amorphous silicon over a substrate;

crystallizing said semiconductor film by irradiating a laser light;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film comprising silicon oxide on each of said first and second semiconductor islands by a vapor phase deposition using TEOS at a temperature of 200 to 400°C.; and

irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas[;].

[forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.]

11. (Four Times Amended) A method for manufacturing a [semiconductor device] thin film transistor comprising the steps of:

forming a semiconductor film comprising amorphous silicon over a substrate;

crystallizing said semiconductor film by irradiating a laser light;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film comprising silicon oxide on each of said first and second semiconductor islands by a vapor phase deposition using TEOS at a temperature of 200 to 400° C.;

irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas; and

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

30. (Four Times Amended) A method for manufacturing a [semiconductor

device] thin film transistor comprising the steps of:

forming a crystalline semiconductor film over a substrate;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film comprising silicon oxide on each of said first and second semiconductor islands by a vapor phase deposition using TEOS at a temperature of 200 to 400° C.;

irradiating an intense light to said insulating film [in an atmosphere comprising an oxygen gas];

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

34. (Four Times Amended) A method for manufacturing a [semiconductor device] thin film transistor comprising the steps of:

forming a crystalline semiconductor film over a substrate;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film comprising silicon oxide on each of said first and second semiconductor islands by a vapor phase deposition using TEOS at a temperature of 200 to 400° C.;

irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas; [and]

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.